10/731,714

Entry is approved. 8/9/06 MR

AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line ~~2,~~ 3 with the following rewritten paragraph: ya 9/14

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which like reference numbers indicate like features and wherein:

Figures 1A and 1B illustrate ~~Figure 1 illustrates~~ the scan testing circuit design for a SoC in accordance with the present invention;

Figures 2 displays the clock control mechanism implemented in the scan testing circuit design of Figure1;

Figures 3 shows the scan enable registering logic of Figure1;

Figure 4 illustrates the clock generator for scan chain group A of Figure 1;

Figure 5 shows the clock generator for scan chain group B of Figure 1;

Figure 6 displays the clock generator for scan chain group C of Figure 1;

Figure 7 illustrates the test mode select arrangement for the test mode delta signal TMΔ of Figure 2;

Figure 8 illustrates the test mode select arrangement for the simultaneous test mode signal TM_{ALL} and intermediate control signals, sig_A, sig_B, and sig_C ~~of Figure 2~~; and

Figure 9 displays the test mode select arrangement for the first, second and third test mode signals, TM_1, TM_2, and TM_3, and the VLCT mode signal $VLCT_M$ of Figure 2.

Please replace the paragraph beginning at page 8, line 23, with the following rewritten paragraph:

Figure 1A ~~1~~ illustrates the scan test circuit design for a mixed signal SoC in accordance with the present invention. For simplicity, Figure 1A ~~1~~ clearly